

REMARKS

Claims 1-15 are pending and rejected in the present application. Claims 1, 8 and 9 are amended, and claim 16 is added, hereby.

Applicants acknowledge the withdrawal of the restriction requirement and rejoinder of claims 1-8.

5 Responsive to the objection to claim 8 on the basis of the informalities noted by the Examiner, Applicants have amended claim 8 and submit that claim 8 is now in allowable form. Accordingly, Applicants respectfully request withdrawal of the objection and allowance of the claim.

10 Claims 1, 5, 6, 8 and 9 were rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,271,097 (Morris). Responsive thereto, Applicants have amended claim 1 and submit that claim 1 is now in condition for allowance.

15 A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference". *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Further, the elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831,

20 15 USPQ2d 1566 (*Fed. Cir. 1990*). Applicants submit that the cited reference fails to disclose each and every limitation of claim 1.

Morris discloses an integrated circuit device wherein collector and emitter mesas 221 and 223 (Fig. 4C), respectively, are formed. In the void or gap between the collector and emitter mesas 221 and 223, a passivation layer 224 and base contact layer 226 are grown and base contacts 228 are formed on
25 layer 226. (*column 7, lines 55-60, Fig. 4E*). Contact layer 226 is then removed from regions not covered by base contacts 228 (Fig. 4E).

In contrast, claim 1 recites in part “forming a third compound semiconductor material upon . . . the exposed first active layer and at least
30 partially within the opening, wherein: the third compound semiconductor material has an upper surface that is substantially co-planar with an upper surface of the second compound semiconductor layer”. (*Emphasis Added*).

The method of Morris forms mesas between which a base contact structure is formed. The present invention, however, utilizes a planar process
35 and forms a planar device. The disadvantages of a mesa-based processes and structures are well known to those of ordinary skill in the art, as are the advantages of a planar-based processes and structures. In fact, the advantages of a planar device are explicitly recognized within Morris at column 8, lines 2-6, wherein it is claimed that the Morris device is “quasi-planar” and thereby provides
40 significant advantages for patterning and etching. Although Applicants are not

certain what constitutes a “quasi-planar” device, it is apparent from the foregoing that the process and structure of Morris is mesa-based and not planar based and it is further apparent that a truly planar process and structure, such as the process and structure of the present invention, is advantageous relative thereto.

45 The base contact structure of Morris is not coplanar with the upper surface of the uppermost active/compound semiconductor layer. Thus, Morris fails to disclose a method for forming a coplanar structure as recited in part by amended claim 1. More particularly, Morris fails to disclose forming a third compound semiconductor material within the opening and having an upper surface that is
50 substantially co-planar with an upper surface of the second compound semiconductor layer, as recited in part by claim 1.

 Moreover, the semiconductor layer deposited between the mesas of the Morris device is not deposited onto the first compound semiconductor (base) layer. Rather, it is deposited onto a passivation layer formed over the first
55 compound semiconductor layer. Thus, Morris also fails to disclose forming a third compound semiconductor material upon the first active layer exposed within the opening, as recited in part by amended claim 1.

 For the foregoing reasons, Applicants submit that Morris fails to disclose each and every limitation of claim 1, and therefore does not anticipate claim 1.
60 Accordingly, Applicants submit that claim 1 and claims 2-8 depending therefrom are now in condition for allowance, which is hereby respectfully requested.

Claim 9 was also rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,271,097 (Morris). Responsive thereto, Applicants have amended claim 9 and submit that claim 9 is now in condition for allowance.

65 Amended claim 9 recites in part “a fourth compound semiconductor material at least partially within the opening, . . . the fourth compound semiconductor material having an upper surface that is substantially coplanar with an upper surface of the third compound semiconductor layer”. (*Emphasis Added*). Thus, in that regard, claim 9 recites subject matter that is substantially
70 similar to the subject matter recited in part by amended claim 1. For the same reasons given above in regard to claim 1, Applicants submit Morris fails to disclose each and every limitation of claim 9, and therefore does not anticipate claim 9. Accordingly, Applicants respectfully requests withdrawal of the rejection and allowance of claims 9 and claims 10-15 depending therefrom.

75 Claims 1, 5, 6, 8, 9, and 12-15 were also rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent No. 5,698,871 (Sakai, et al.). Responsive thereto, Applicants have amended claim 1 and submit that claim 1 is now in condition for allowance.

Claim 1 as amended recites in part “forming a third compound
80 semiconductor material upon at least a portion of the exposed first active layer and at least partially within the opening, wherein: the third compound semiconductor material has an upper surface that is substantially co-planar with

an upper surface of the second compound semiconductor layer". (*Emphasis Added*).

85 In contrast, the device of Sakai, et al. forms base contacts 16 (Fig. 5(g))
on base layer 4 between regrown crystal layers 14 and 15 and sidewalls 12 of a
mesa transistor structure. Because the device of Sakai, et al., is a mesa-based
structure, the base contacts 16 must extend above emitter layer 5 and above
regrown layer 14. The base contacts 16 of Sakai, et al., are not coplanar with the
90 emitter layer 5. Thus, Sakai, et al., fails to disclose or suggest forming a third
compound semiconductor material upon at least a portion of the exposed first
active layer and at least partially within the opening having an upper surface that
is substantially co-planar with an upper surface of the second compound
semiconductor layer, as recited in part by amended claim 1.

95 For the foregoing reasons, Applicants submit that Sakai, et al., fails to
disclose each and every limitation of claim 1, and therefore does not anticipate
claim 1. Accordingly, Applicants submit that claim 1 and claims 2-8 depending
therefrom are now in condition for allowance, which is hereby respectfully
requested.

100 Claims 9 and 12-15 were also rejected under 35 U.S.C. §102(b) as being
unpatentable over U.S. Patent No. 5,698,871 (Sakai, et al.). Claim 9 has been
amended to recite in part "a fourth compound semiconductor material at least
partially within the opening, . . . the fourth compound semiconductor material

having an upper surface that is substantially coplanar with an upper surface of the third compound semiconductor layer". (*Emphasis Added*). Thus, in that regard, claim 9 recites subject matter that is substantially similar to the subject matter recited in part by amended claim 1. For the same reasons given above in
5 regard to claim 1, Applicants submit that Sakai fails to disclose each and every limitation of amended claim 9, and therefore does not anticipate claim 9. Accordingly, Applicants respectfully requests withdrawal of the rejection and allowance of claims 9 and claims 10-15 depending therefrom.

Claims 3, 4, 7, 10 and 11 were rejected under 35 U.S.C. §103(a) as being
10 unpatentable over U.S. Patent No. 6,271,097 (Morris) in view of U.S. Patent No. 6,329,675 (Singh, et al.). Applicants respectfully point out that claims 3, 4 and 7 depend from claim 1, which is in condition for allowance for the reasons provided herein. Further, Applicants respectfully point out that claims 10 and 11 depend from claim 9, which is also in condition for allowance for the reasons provided
15 herein. Accordingly, Applicants submit that claims 3, 4, 7, 10 and 11 are also now in condition for allowance and respectfully request same.

Claims 3, 4, 7, 10 and 11 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,698,871 (Sakai, et al.) in view of U.S. Patent No. 6,329,675 (Singh, et al.). Applicants respectfully point out that claims 3, 4
20 and 7 depend from claim 1, which is in condition for allowance for the reasons provided herein. Further, Applicants respectfully point out that claims 10 and 11

depend from claim 9, which is also in condition for allowance for the reasons provided herein. Accordingly, Applicants submit that claims 3, 4, 7, 10 and 11 are also now in condition for allowance and respectfully request same.

Claim 2 was rejected under 35 U.S.C. §103(a) as being unpatentable
5 either Morris/Singh or alternatively Sakai/Singh as applied to claim 1 and further in view of Luo, et al., "Demonstration of 4H-SiC Power Bipolar Junction Transistors", Electronic Letters, 17th August 2000, Vol. 36, No. 17, pp. 1496-1497. Applicants respectfully point out that claim 2 depends from claim 1, which is in condition for allowance for the reasons provided herein. Accordingly,
10 Applicants submit that claim 2 is also now in condition for allowance and respectfully request same.

Claim 16 has been added hereby to further protect the patentable subject matter of the present invention. Claim 16 recites in part:

15 "an opening . . . extending through the third active layer [and] terminating within and exposing a portion of the second active layer, sidewalls of the opening formed by the third active layer, a bottom of the opening formed by the exposed portion of the second active layer; an insulating layer at least partially within the opening and covering the sidewalls thereof; and a fourth compound semiconductor material disposed within the opening upon the exposed portion of the second active layer and upon the insulating layer covering the sidewalls thereof, . . . the fourth compound semiconductor material substantially filling the opening and having an upper surface that is substantially coplanar with an upper
20 surface of the third compound semiconductor layer.
25

(Emphasis Added).

As discussed above, Applicants submit that none of the cited references disclose or suggest, alone or in combination, all the limitations of claim 16. Accordingly, Applicants submit that claim 16 is in condition for allowance and respectfully request same.

5 For all the foregoing reasons, Applicants submit that the amended claims are definite and do particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Further, Applicants submit that no combination of the cited references teaches, discloses or suggests the subject matter of the amended claims. The pending claims are therefore in allowable
10 form and in condition for allowance. Accordingly, Applicants respectfully request withdrawal of all rejections and allowance of the claims.

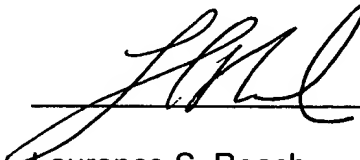
In the event Applicants have overlooked the need for an extension of time, an additional extension of time, payment of fee or additional payment of fee, Applicants hereby conditionally petitions therefor.

The Examiner is invited to telephone the undersigned in regard to this
Amendment and the above identified application.

Respectfully submitted,

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Date



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